SEMICONDUCTORS

# ANSYS RedHawk-SC

## Next-Generation SoC Power Integrity and Reliability Signoff

***ANSYS simulation technology enables you to predict with confidence that your products will thrive** in the real world. Chip-Package-System design engineers trust our software to ensure the integrity **of their products and drive business success through innovation.***

ANSYS® RedHawk-SC™ is the next-generation SoC power noise signoff platform designed to enable sub-16nm design success. RedHawk-SC is built on ANSYS® SeaScape™, the world's first custom designed big data architecture for electronic system design and simulation. ANSYS SeaScape provides per-core scalability, flexible design data access, instantaneous design bring-up, MapReduce-enabled analytics and many other revolutionary capabilities. ANSYS® RedHawk™, the industry's gold standard platform for SoC power noise and reliability signoff is offered on the SeaScape platform as RedHawk-SC, thus giving you the best of both worlds — the signoff confidence RedHawk provides and the elastic scalability and big data analytics of ANSYS SeaScape.

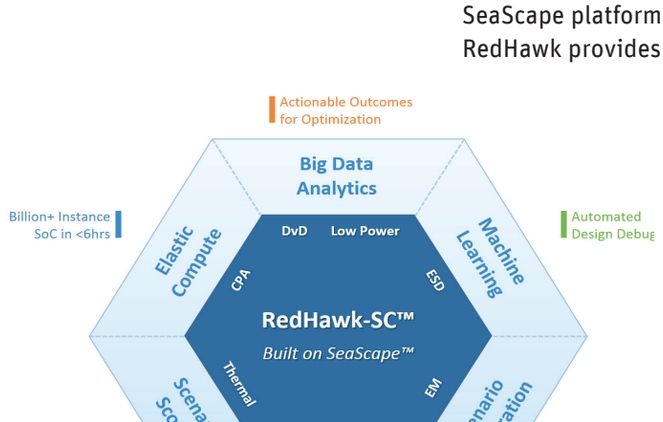


*Figure 1: RedHawk-SC™ Platform*

### Elastic Compute Scalability

With unparalleled scalability across thousands of cores using big data techniques, ANSYS RedHawk-SC helps you sign off billion+ instance designs within a few hours on commodity hardware. No dedicated machines are needed — RedHawk-SC runs the largest designs, using low memory cores, even if they reside on different machines.

When RedHawk-SC launches, it starts working as soon as a single core is available. It proportionately speeds up as more cores become available, and has the resiliency to recover should any core or machine become unresponsive. Because RedHawk-SC can utilize unused cores, it increases utilization rates of compute farms, thereby decreasing overall hardware costs; unlike other tools it does not require dedicated hardware, even for the largest designs.

This elastic scalability is what enables RedHawk-SC to process designs of unprecedented size with flat accuracy, high resolution extracted networks and multiple scenarios.

### Big Data Analytics

Big data analytics enable rapid data mining and analytics to drive actionable outcomes and optimization. Using custom data analytics, you can identify and prioritize only those design fixes that are key to product success. Custom analytics powered by MapReduce enable you to query the largest designs in minutes. RedHawk-SC offers combined display and analytics across multiple views; heat maps for design quality check analysis; combined analysis across multiple scenarios for coverage analysis and issue diagnostics; and custom heat-map support.

### Accelerated Design Closure

With the increasing number of cores in CPU and GPU sub-systems in next-generation SoCs, it is crucial to understand and isolate the switching combination that can generate a chip-package-PCB resonance condition resulting in catastrophic voltage-drop-induced failure. RedHawk-SC leverages patented algorithmic approaches customized on the SeaScape architecture to perform rapid design evaluation by exploring thousands of switching possibilities, and highlighting specific operating modes that should be avoided either through design or software level changes.

Design teams often struggle with understanding which vectors to use and which cycles within these vectors to simulate for signoff. Using RedHawk-SC's multiphysics analytics, you can now "score" vectors across multiple parameters to identify the appropriate vectors and, more crucially, isolate cycles within these vectors that are important for power noise signoff. This will help you perform targeted simulations while getting meaningful coverage.

## Multiphysics Optimization

For advanced process nodes, margin-based design methodologies force overdesign and guardbanding, resulting in larger die sizes and increased design schedules. With RedHawk-SC you can perform multi-scenario simulations and run multiphysics analytics all within your design ECO cycle. With this methodology, you can target fixes in high stress areas while reducing overdesign in other parts of the chip. The design fix suggestions can be done quickly and efficiently through standard interfaces with existing place and route solutions. This has been proven over multiple successful tapeouts to reduce power consumption and die size while meeting performance and reliability targets.

## Multi-site Collaboration using Thin Client Support

RedHawk-SC is built for multi-site collaboration and effective design analysis. Users across multiple sites can simultaneously view, debug and explore design and simulation results. You can bring up the largest designs in small memory machines in minutes and simultaneously view and optimize the same database across multiple sites.

## Instantaneous Result and Native Layout Viewing with Full Hierarchical Support

RedHawk-SC allows simultaneous power and signal line analysis on a full-chip SoC with full hierarchical support. You can interactively view and monitor progress of the analysis while simulation is ongoing. You can also debug results with current heat maps that display nodes/edges for clear identification of the extracted circuit for advanced current flow and EM modeling.

## Machine Learning Support

Machine learning support enables a wide range of applications, such as identifying missed systematic design weaknesses and automating time-consuming rigorous manual procedures. This is done by aggregating key insights across different designs using continuing and prior simulation and design data.

## Comprehensive Dynamic Analysis Coverage

RedHawk-SC offers you the most comprehensive dynamic analysis coverage by enabling you to sign off SoCs with confidence using a wide variety of simulation modes — RTL and gate vectors; smart VectorLess analysis for functional and scan mode; mix-mode simulation (vectorless + VCD); and frequency-aware vectorless to stress system level PDN, power-transient and power-up analysis.

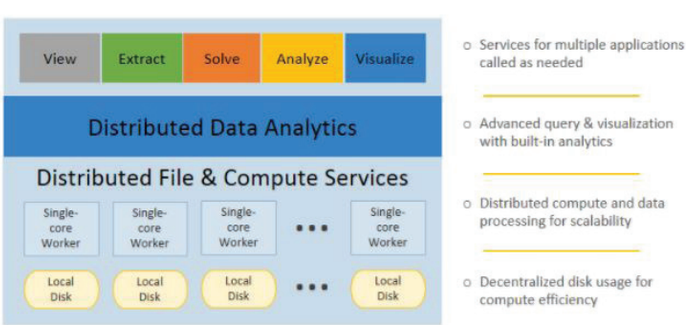


*Figure 2: RedHawk-SC Architecture*

## Chip Package Co-optimization

You can perform chip-package co-optimization by modeling the package and board for system-aware chip signoff and enabling chip power modeling for chip-aware system signoff.

## Electromigration and ESD Signoff

RedHawk-SC offers comprehensive electrostatic discharge (ESD) analysis of HBM and CDM ESD events and power and signal electromigration (EM) analysis, in addition to advanced thermal-aware EM and statistical EM budgeting, which is a pressing reliability problem for sub-16nm designs.

## Silicon-proven Signoff Leader

As the industry's most silicon-proven SoC power integrity and reliability signoff solution, supported by certifications from all foundries for every manufacturing process technology down to 7nm, ANSYS delivers the accuracy of its new RedHawk-SC for SoC signoff success.

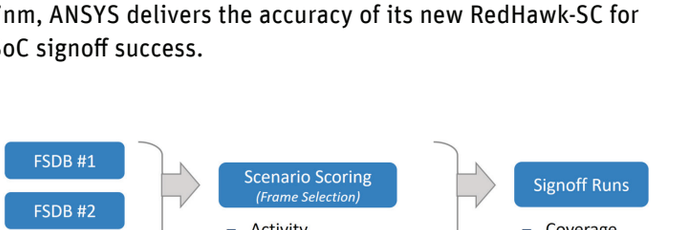


*Figure 3: Critical vector selection based on multiple different parameters*

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