RedHawk platform enables power noise closure and sign-off for low-power, high-performance SoCs using sub-20nm FinFET and other advanced technologies. RedHawk's advanced engines and simulation capabilities delivers significantly higher capacity and improved analysis turn-around times (TAT) for full-chip IR/dynamic voltage drop (DvD), power/signal electromigration (EM) and electro-static discharge (ESD) analyses. It enables early design prototyping, RTL-to-GDS power closure, SoC-level IP verification, integrated package analysis, and chip-aware system analyses.

RedHawk's extraction, simulation and EM/ESD engines have been certified by multiple foundries and have been silicon validated on sub-20nm designs. With 1000s of successful tape-outs, RedHawk is used by all of the top 20 semiconductor companies in the world to meet the increasing constraints of power-performance-price targets for their designs.

**KEY CAPABILITIES**

- SPICE accurate transient simulation results at the SoC level using dynamic power models
- 3X faster turn-around time using advanced extraction and simulation engines
- Out-of-box VectorLess algorithm for quick dynamic hot-spot identification and sign-off coverage
- Advanced logic simulation engine for complete RTL-to-GDS sign-off
- Integrated next-generation root cause identification and debugging using RedHawk Explorer (RHE)
- Versatile environment for power grid prototyping and design optimization
- Package/PCB-aware SoC sign-off with full support for RLCK and S-parameter package models
High Capacity and Performance

RedHawk delivers 3X faster turn-around time compared to its previous version by using advanced extraction and simulation engines that leverage the state-of-art software architecture for high-throughput multi-CPU computing. In addition to performance improvements, the latest version of RedHawk reduces its corresponding peak memory footprint and disk-space usage.

RedHawk’s best-in-class transient simulation engine can handle 1B+ nodes of RLC network matrices along with fully distributed and cross-coupled package models. By performing full-chip flat analyses, RedHawk maintains its sign-off accuracy for dynamic voltage drop, EM and ESD.

Silicon Validated Sign-off Accuracy

RedHawk provides SPICE accurate transient simulation results at the SoC level using dynamic power models for standard cells and analog/custom IPs. It uses these models to simultaneously simulate all the power and ground domains and to predict the current drawn and voltage seen at every cell in the design.

RedHawk accuracy simulates the effect of package and PCB parasitics on DvD noise inside the chip and supports lumped and distributed models represented in RLCK and S-parameter formats. RedHawk also includes on-die power delivery network (PDN) RLC extraction engine that has been re-architected and certified for sub-20nm technologies.

RTL-to-GDS Power Noise Closure

RedHawk uses advanced logic simulation engine for complete RTL-to-GDS sign-off. It allows for multiple different ‘excitation’ modes, including ‘mixed-mode’ simulation where different parts of the design can leverage whatever data is available.

RedHawk’s out-of-box VectorLess algorithm enables quick dynamic hot-spot identification and sign-off coverage without requiring input vectors. The ‘multi-scenario’ mode in RedHawk VectorLess simulation allows a designer to cycle through multiple different activity modes, without requiring additional input.

Advanced Reliability Sign-off Analysis

RedHawk is foundry certified for power EM, signal EM and SoC ESD analysis and sign-off. It provides full support for both power/ground and signal line EM analyses. Along with PathFinder engine, RedHawk provides SoC-level connectivity and failure check analyses for all current flow pathways (wires, vias) from an ESD event (HBM, CDM).

Results Analysis and Root Cause Identification

RedHawk’s multi-tab, multi-pane GUI allows for faster debug and results analysis by simultaneously displaying various results and tables. RedHawk Explorer, an integrated root-cause identification and debugging tool provides data integrity, design weakness and hot-spot analyses information, as well as feedback on how to improve simulation turn-around time.

Low Power Design Verification

RedHawk supports simulation and analysis of complex low-power design techniques such as clock gating, power gating, on-chip regulators and adaptive back-bias networks. It can simultaneously simulate the various voltage islands in a chip, while considering the coupling effects that can be detrimental. RedHawk’s VectorLess engine can model the various operating and transition modes of the clock tree network so that engineers can predict the effects of transient current on the clock tree and chip performance.
Impact on Timing Analysis

RedHawk helps understand the impact of DvD on timing for clock and critical path. This integrated capability allows engineers to perform fast full-chip level timing impact analysis to identify the areas of concern, followed by a SPICE based sign-off simulation on those affected path(s) and clock tree(s).

System-aware Chip and Chip-aware System Analyses

RedHawk enables the creation of Chip Power Model (CPM) which revolutionized chip-package-system (CPS) co-design and co-analyses. CPM captures all the electrical characteristics of a chip including switching current, parasitics (resistance, capacitance and inductance) in a compact, open SPICE format that can be used by package/PCB level power integrity, EMI and thermal analyses.

RedHawk supports package and PCB models in various industry standard formats and varying complexities. The package models created using any industry standard solutions such as Sentinel-PSI or ANSYS SIwave can be directly imported into RedHawk, enabling system-aware chip analysis.