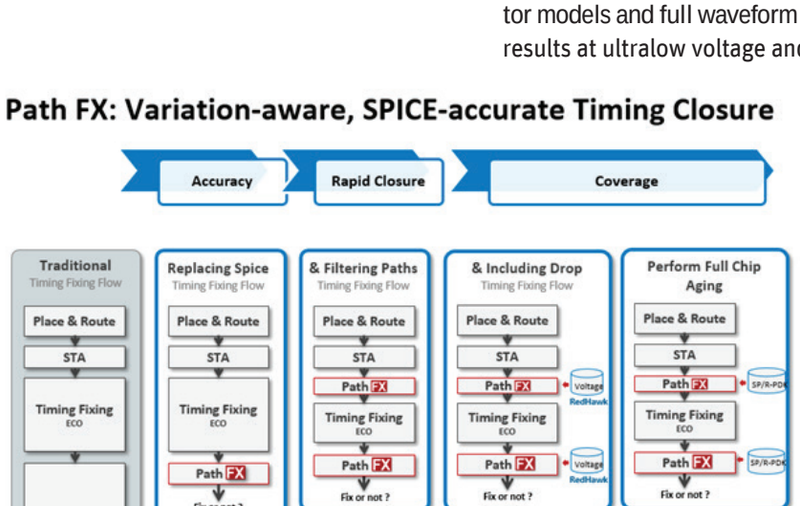
ANSYS Path FX™

ANSYS® Path FX™ is a critical path analysis tool that complements existing static timing analysis sign-off tools. It can evaluate hundreds of thousands of timing paths and clock trees in an SoC for delay and variance for even the largest designs. Path FX has production-proven, SPICE-like accuracy to tackle the most advanced manufacturing processes, and the functionality to account for all critical contributors to delay and constraints across multiple process, voltage, temperature corners and scenarios.

Path FX makes it practical to calculate timing with variation on a full SoC without taking any shortcuts. With a fully threaded and distributed architecture and the ability to run on thousands of CPUs, turnaround time scales inversely with the number of CPUs available.



Accurate Path-based Critical Path Timing

Path FX can simulate thousands of paths using standard cell models or transistor-level SPICE models, providing both corner and statistical timing results. It leverages the SPICE transistor models and full waveform propagation to provide the accuracy needed to get reliable results at ultralow voltage and advanced processes. Miller-capacitance and other effects are handled correctly, with no shortcuts to simulate delays, slews and constraints. The simulator is fully statistical and handles non-Gaussian behavior at low voltage and advanced process nodes. Path FX is threaded and distributed, dramatically reducing turnaround time and memory requirements, compared to Monte Carlo SPICE.

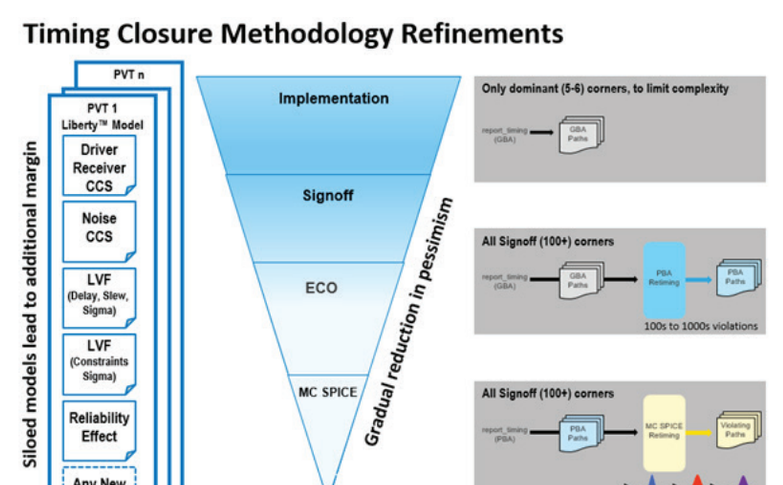
Rapid Design Closure

The increasing complexity of electrical effects such as signal integrity, on-chip variation (OCV), statistical OCV, etc., has made constant enhancement of the industry-standard Liberty™ library model necessary. A siloed addition of such effects has led to the introduction of additional margins in the model. Methodologies ensure gradual reduction of pessimism from design implementation to Monte Carlo SPICE, but there's potential overdesign that can be minimized. Design implementation limits complexity by using graph-based analysis (GBA) for faster turn-around time (TAT) and coarse timing closure. In contrast, signoff static timing analysis (SSTA) uses more accurate path-based analysis (PBA) techniques to ensure all critical paths have been checked. Finally, Monte Carlo SPICE is run on a limited set of paths to identify real violations and waive the rest.

Path FX improves such margin-based methodologies through fast and high capacity transistor-accurate analysis to rapidly identify the real violations, reducing days of engineering change orders (ECO) down to hours. Path FX reads industry standard files and generates a rich set of reports and standard delay format (SDF) for back-annotating results into your flow.

Coverage

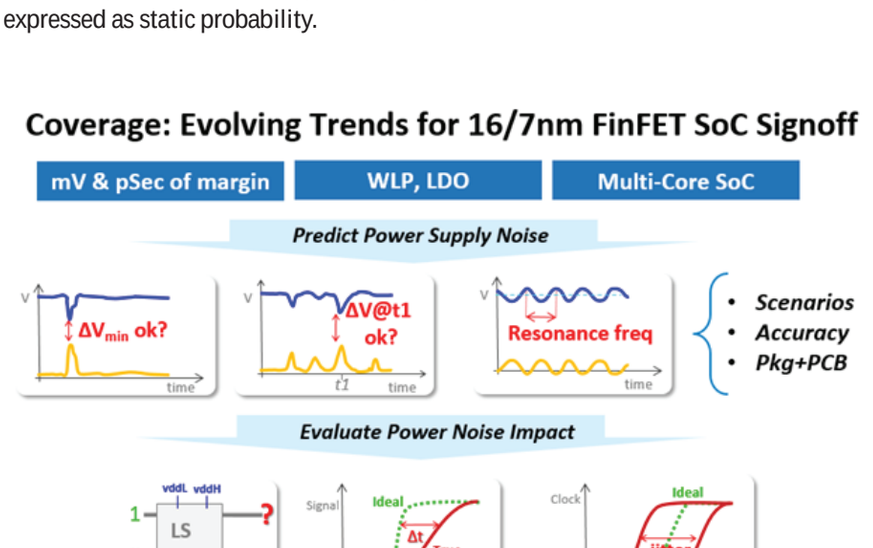
As geometries have shrunk, operating voltage has also scaled down to meet low-power needs for mobile applications, or thermal requirements for packages for high performance computing and automotive applications. However, threshold voltages of transistors have not scaled proportionately. This has led to an increased sensitivity to voltage drop. At sub-16nm, transistor delays can change significantly due to dynamic voltage drop (DvD).



In addition to simulating timing paths, Path FX automatically identifies and simulates every clock path in your design. Further, Path FX accounts for accurate multi-voltage analysis, and performs accurate DvD-aware timing and clock jitter analysis.

Finally, at sub-16nm geometries the stress effect of high electric fields across the dielectric have resulted in worse aging behavior. This is primarily due to negative bias temperature instability (NBTI), which causes the threshold voltage of the transistor to degrade, leading to lower switching speeds. This effect depends on the activity level of the circuits, with heavier impact on parts of the design that don't switch as often (gated clocks, control logic, and reset, programming and test circuitry).

Path FX™ performs instance-specific aging simulations that accurately account for workloads, expressed as static probability.



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